IN THE CLAIMS

This listing of the claim will replace all prior versions and listings of claim in the present application.

Listing of Claims

1. (original) A nonvolatile memory apparatus comprising;

a plurality of terminals including a clock terminal, a command terminal and other terminal;

a first buffer;

a second buffer; and

a plurality of nonvolatile memory cells,

wherein said clock terminal receives a clock signal,

wherein said command terminal couples to said second buffer and receives commands which include a read command and a program command.

wherein said first buffer is used for receiving data from outside of said nonvolatile memory apparatus and is used for outputting data to outside of said nonvolatile memory apparatus,

wherein in an operation in response to said read command received from said command terminal, said nonvolatile memory apparatus reads data from ones of said nonvolatile memory cells, stores read data to said first buffer, and outputs said read data stored in said first buffer to outside of said nonvolatile memory apparatus via said other terminal not said command terminal in response to said clock signal, and

wherein in an operation in response to said program command, said nonvolatile memory apparatus receives data from outside of said nonvolatile memory

apparatus via said other terminal not said command terminal in response to said clock signal, stores received data to said first buffer and writes said received data stored in said first buffer to ones of said nonvolatile memory cells.

2. (original) A nonvolatile memory apparatus according to claim 1, further comprising:

a decode circuit,

wherein said decode circuit decodes said commands received in said second buffer.

3. (currently amended)A nonvolatile memory apparatus ~~according to claim 2~~, comprising;

a plurality of terminals including a clock terminal, a command terminal and other terminal;

a first buffer;

a second buffer;

a plurality of nonvolatile memory cells; and

a decode circuit,

wherein said clock terminal receives a clock signal,

wherein said command terminal couples to said second buffer and receives commands which include a read command and a program command.

wherein said first buffer is used for receiving data from outside of said nonvolatile memory apparatus and is used for outputting data to outside of said

nonvolatile memory apparatus,

wherein in an operation in response to said read command received from said command terminal, said nonvolatile memory apparatus reads data from ones of said nonvolatile memory cells, stores read data to said first buffer, and outputs said read data stored in said first buffer to outside of said nonvolatile memory apparatus via said other terminal not said command terminal in response to said clock signal,

wherein in an operation in response to said program command, said nonvolatile memory apparatus receives data from outside of said nonvolatile memory apparatus via said other terminal not said command terminal in response to said clock signal, stores received data to said first buffer and writes said received data stored in said first buffer to ones of said nonvolatile memory cells,

wherein said decode circuit decodes said commands received in said second buffer,

wherein each of said nonvolatile memory cells has a threshold voltage an arbitrary one of a plurality of threshold voltage ranges,

wherein said threshold voltage ranges include a threshold voltage range indicating an erase state and a threshold voltage range indicating a program state, and

wherein said nonvolatile memory apparatus controls moving said threshold voltage of one nonvolatile memory cell to within one of threshold voltage ranges indicating said program state, and keeping said threshold voltages of remaining nonvolatile memory cells of ones of said nonvolatile memory cells within said threshold voltage range indicating said erase state, in said operation in response to

said program command.

4. (original) A nonvolatile memory apparatus according to claim 3, wherein said commands further include an erase command,

wherein in an operation in response to said erase command received from said command terminal, said nonvolatile memory apparatus erases data stored in ones of said nonvolatile memory cells, and

wherein said nonvolatile memory apparatus controls moving said threshold voltages of ones of said nonvolatile memory cells to within said threshold voltage range indicating said erase state in said operation in response to said erase command.

5. (currently amended)A nonvolatile memory apparatus according to claim ~~1~~4, further comprising:

a circuit,

wherein in said operation in response to said read command, said circuit senses status of data according to a threshold voltage of a nonvolatile memory cell which is within whether said threshold voltage range indicating said erase state or said threshold voltage range indicating said program state.

6. (original) A nonvolatile memory apparatus according to claim 5, wherein said other terminal is a data terminal,

wherein said data terminal receives data in said operation in response to said

program command, and

wherein said data terminal outputs data in said operation in response to said read command.

7. (currently amended)A nonvolatile memory apparatus comprising;

a plurality of terminals including a clock terminal, a command terminal and other terminal;

a first buffer;

a second buffer;

a plurality of nonvolatile memory cells; and

a decode circuit,

wherein said clock terminal receives a clock signal,

wherein said command terminal couples to said second buffer and receives commands which include a read command and a program command.

wherein said first buffer is used for receiving data from outside of said nonvolatile memory apparatus and is used for outputting data to outside of said nonvolatile memory apparatus,

wherein in an operation in response to said read command received from said command terminal, said nonvolatile memory apparatus reads data from ones of said nonvolatile memory cells, stores read data to said first buffer, and outputs said read data stored in said first buffer to outside of said nonvolatile memory apparatus via said other terminal not said command terminal in response to said clock signal,

wherein in an operation in response to said program command, said

nonvolatile memory apparatus receives data from outside of said nonvolatile memory apparatus via said other terminal not said command terminal in response to said clock signal, stores received data to said first buffer and writes said received data stored in said first buffer to ones of said nonvolatile memory cells,

wherein said decode circuit decodes said commands received in said second buffer, ~~according to claim 2~~,

wherein each of said nonvolatile memory cells has a threshold voltage within an arbitrary one of a plurality of threshold voltage ranges,

wherein said threshold voltage ranges include a threshold voltage range indicating an erase state and a plurality of threshold voltage ranges each indicating a corresponding program state, and

wherein said nonvolatile memory apparatus controls moving said threshold voltage of one nonvolatile memory cell to within one of said threshold voltage ranges indicating said program states according to data, and keeping said threshold voltages of remaining nonvolatile memory cells of ones of said nonvolatile memory cells, in said operation in response to said program command.

8. (original) A nonvolatile memory apparatus according to claim 7, wherein said commands further include an erase command,

wherein in an operation in response to said erase command received from said command terminal, said nonvolatile memory apparatus erases data stored in ones of said nonvolatile memory cells, and

wherein said nonvolatile memory apparatus controls moving threshold

voltages of ones of said nonvolatile memory cells to within said threshold voltage range indicating said erase state in said operation in response to said erase command.

9. (original) A nonvolatile memory apparatus comprising:

a first volatile memory;

a second volatile memory;

a clock terminal;

a data terminal;

a command terminal; and

a plurality of nonvolatile memory cells,

wherein said clock terminal receives a clock signal,

wherein said data terminal couples to said first volatile memory,

wherein said command terminal couples to said second volatile memory and receives commands which include a read command and a program command,

wherein in an operation in response to said read command received from said command terminal, said nonvolatile memory apparatus reads data from ones of said nonvolatile memory cells, is capable of transferring data to said first volatile memory, and serially outputs data from said first volatile memory via said data terminal in response to said clock signal, and

wherein in an operation in response to said program command received from said command terminal, said nonvolatile memory apparatus receives data in said first volatile memory via said data terminal in response to said clock signal, transfers

data from said first volatile memory and writes data to ones of said nonvolatile memory cells.

10. (original) A nonvolatile memory apparatus according to claim 9, further comprising:

a decode circuit,

wherein said decode circuit decodes said commands received in said second volatile memory.

11. (original) A nonvolatile memory apparatus according to claim 10, wherein each of said nonvolatile memory cells has a threshold voltage within an arbitrary one of a plurality of threshold voltage ranges,

wherein said threshold voltage ranges include a threshold voltage range indicating an erase state and a threshold voltage range indicating a program state, and

wherein said nonvolatile memory apparatus controls moving said threshold voltage of one nonvolatile memory cell to within said threshold voltage range indicating said program state and keeping threshold voltages of remaining nonvolatile memory cells of said nonvolatile memory cells within said threshold voltage range indicating said erase state, in said operation in response to said program command.

12. (original) A nonvolatile memory apparatus according to claim 11,

wherein said commands further include an erase command,

wherein in an operation in response to said erase command received from said command terminal, said nonvolatile memory apparatus erases data stored in ones of said nonvolatile memory cells, and

wherein said nonvolatile memory apparatus controls moving said threshold voltages of ones of said nonvolatile memory cells to within said threshold voltage range indicating said erase state in said operation in response to said erase command.

13. (original) A nonvolatile memory apparatus according to claim 12, further comprising:

a circuit,

wherein in said operation in response to said read command, said circuit senses status of data according to a threshold voltage of said nonvolatile memory cell which is within whether said threshold voltage range indicating said erase state or said threshold voltage range indicating said program state.

14. (original) A. nonvolatile memory apparatus according to claim 10, wherein each of said nonvolatile memory cells has a threshold voltage within an arbitrary one of a plurality of threshold voltage ranges,

wherein said threshold voltage ranges include a threshold voltage range indicating an erase state and a plurality of threshold voltage ranges each indicating a corresponding program state, and

wherein said nonvolatile memory apparatus controls moving said threshold voltage of one nonvolatile memory cell to within one of said threshold voltage ranges indicating a corresponding program state according to data and keeping said threshold voltages of remaining nonvolatile memory cells of ones of said nonvolatile memory cells, in said operation in response to said program command.

15. (original) A nonvolatile memory apparatus according to claim 14, wherein said command further include an erase command,

wherein in an operation in response to said erase command, said nonvolatile memory apparatus erases data stored in ones of said nonvolatile memory cells, and

wherein said nonvolatile memory apparatus controls moving threshold voltages of ones of said nonvolatile memory cells to within said threshold voltage range indicating said erase state in said operation in response to said erase command.